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9. (Amended) A computer-readable memory containing computer-executable program instructions comprising instructions for:

generating a physically-accurate description of a first portion of an electronic system, said physically-accurate description comprising actual physical characteristics of said first portion;

generating an approximate mathematical model of a remaining portion of said system, said model being based upon hierarchical analysis of said remaining portion; and

simulating operation of said system using both said description and said model.

REMARKS

This Amendment is filed in response to the Office Action mailed on July 3, 2002. All objections and rejections are respectfully traversed.

Claims 1-12 are in the case.

Claims 1, 5, 9 were amended to better claim the invention.

At Paragraph 2 of the Office Action the drawings were objected to. Formal drawings will be filed in due course.

At Paragraph 3 of the Office Action the Claims were rejected under 35 U.S.C. 102(b) as being anticipated by McDonald et al., "Timing Analysis for the PA 8000", EE Design, February 1997 (downloaded text from www.eedesign.com/editorial/1997/coverstory9702.html).

The present invention, as set forth in representative claim 1, comprises in part:

> 1. A computerized method for use in simulating an operation of an electronic system, said method being carried out using a computer system, said method comprising the steps of:
>
> generating ***a physically-accurate description of a first portion of said system,*** said physically-accurate description comprising actual physical characteristics of said first portion;
>
> ***generating an approximate mathematical model of a remaining portion of said system,*** said model being based upon hierarchical analysis of said remaining portion; and
>
> using both said physically-accurate description and said approximate model to simulate the operation of said system.

McDonald discloses a computer program called PathMill. The computer program does timing calculations for a simulated electronic circuit. The computer program has a number of characteristics, including:

PathMill generates an abstraction of a block, called a gray box, which contains only the worst case timing arcs between latches and ports. Using a gray box for each major block in a full-chip model reduces the amount of data for simulation.

PathMill may contain an integration of gray boxes, transistors, and RC parasitics. This flexibility provides an elegant structure for timing verification of hierarchial designs.

Data flow.

The data flow in this timing methodology is bi-directional. Detailed timing information from low-level blocks is pushed upward, while context information from the top level is pushed down. Low-level blocks are simulated and analyzed with PathMill before generation of gray box models, which are incorporated into the top-level timing model. Block context information is determined at the top level and returned for the next iteration of lower level block simulation and gray box generation.

For tightly coupled blocks, we introduce a level of hierarchy called minichip. At this level, the gray boxes of child blocks are instantiated along with any transistors and RC parasitics that were not abstracted at the lower levels. As in the block analysis, a minichip gray box is generated and submitted for use in the top-level timing model.

The top level netlist contains a mixture of RC parasitics form the global route; transistors for simple structures, such as signal repeaters; and gray boxes for top-level blocks and minichips.

Applicant respectfully urges that Applicant's claimed novel ***generating an approximate mathematical model of a remaining portion of said system*** is not disclosed by McDonald.

Further, Applicant respectfully urges that McDonald explains his "gray boxes" as follows:

"PathMill generates an abstraction of a block, called a gray box, which contains only the worst case timing arcs between latches and ports."

That is, McDonalds "gray box" contains only the worst case timing arcs between latches and ports. In sharp contrast, Applicants disclose and claim the use of a mathematical model of a portion of their system, along with ***a physically-accurate description of a first portion of said system*** and couple the mathematical model and physically accurate description of another portion of their system to generate the full analysis of their system.

Carrying the argument further, McDonalds gray boxes are simply worst case timing arcs, whereas Applicants' claimed mathematical models are an approximate model of their portion of the system, and so are totally different from McDonalds crude gray boxes.

Further, McDonald's minichips are simply combinations of gray boxes. That is, minichips are simply combinations of worst case timing arcs. Accordingly, combining his gray boxes does not enable McDonald to disclose Applicant's claimed mathematical model of a portion of Applicants' system.

Stated differently, Applicant discloses and claims a mathematical model of a portion of their system, where McDonald only discloses a crude worst case timing arc.

Applicant respectfully urges that the McDonald disclosure is legally insufficient to anticipate Applicant's claimed mathematical model under 35 U.S.C. 102(b) because of the absence from McDonald's disclosure of Applicants' claimed ***mathematical model***.

All independent claims are believed to be in condition for allowance.

All dependent claims are believed to be dependent from allowable independent claims, and therefore in condition for allowance.

Favorable action is respectfully solicited.

Please charge any additional fee occasioned by this paper to our Deposit Account No. 03-1237.

Respectfully submitted,

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MARK-UP PAGES FOR THE OCTOBER 1, 2002, AMENDMENT TO U.S. PATENT APPLICATION SER. NO. 09/384,504

The replacement for the FIRST full paragraph of page PAGE resulted from the following changes:

COPY PARAGRAPH TO BE AMENDED HERE.

The replacement for claim CLAIM resulted from the following changes:

COPY CLAIM TO BE AMENDED HERE.

(1)

1. (Amended) A computerized method for use in simulating an operation of an electronic system, said method being carried out using a computer system, said method comprising the steps of:

generating a physically-accurate description of a first portion of said system, said physically-accurate description comprising actual physical characteristics of said first portion;

generating an approximate mathematical model of a remaining portion of said system, said model being based upon hierarchical analysis of said remaining portion; and

using both said physically-accurate description and said approximate model to simulate the operation of said system.

5. (Amended) A computerized system for use in simulating an operation of an electronic system, comprising the steps of:

a modeling engine that modifies a first model of said electronic system, said first model including only hierarchical analysis mathematical functions estimating operation of

said electronic system, said modeling engine modifying said first model to include both at least one hierarchical analysis mathematical function estimating operation of a portion of said electronic system and a physically-accurate description of another portion of said electronic system; and

a simulation engine that simulates the operation of said electronic system based upon both said at least one function and said physically-accurate description.

9. (Amended) A computer-readable memory containing computer-executable program instructions comprising instructions for:

generating a physically-accurate description of a first portion of an electronic system, said physically-accurate description comprising actual physical characteristics of said first portion;

generating an approximate mathematical model of a remaining portion of said system, said model being based upon hierarchical analysis of said remaining portion; and

simulating operation of said system using both said description and said model.